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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/434,736	11/02/1999	SANG YOUNG KIM	000939-07360	4305

20350 7590 03/14/2002

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EXAMINER

PERT, EVAN T

ART UNIT	PAPER NUMBER
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2829

DATE MAILED: 03/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/434,736

Applicant(s)

KIM ET AL.

Examiner

Evan T. Pert

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28,30-39,41-43,45-70,72-80 and 82-88 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

- 5) ☐ Claim(s) _____ is/are allowed.

- 6) ☒ Claim(s) 1-28,30-39,41-43,45-70,72-80 and 82-88 is/are rejected.

- 7) ☐ Claim(s) _____ is/are objected to.

- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☒ Interview Summary (PTO-413) Paper No(s). 16.
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-28, 30-39, 41-43, 45-70, 72-80 and 82-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art [AAPA] (as depicted in Figs. 1A and 1B of U.S. Patent 5,683,938) in view of Gutierrez (U.S. Patent 5,069,749) taken together with Wolf (Textbook Chapter 4 Entitled "MULTILEVEL-INTERCONNECT TECHNOLOGY").

Claims 1-28, 30-39, 41-43, 45-63 [Method Claims]

Referring to applicant's Figs. 1A and 1B, and the corresponding explanatory text, AAPA comprises a methodology for forming a semiconductor device DRAM structure having a conductive gate 5, gate insulator 4, field oxide layer 3, source and drain junction regions 2 (inherently P+ doped for an n-channel by Official Notice), silicon substrate 1, first insulating layer 6 and second insulating layer 8, as well as poly line 7 on the 1st ILD layer 6.

The vias 20 in AAPA are filled *after* the first *and* second insulating layers are formed, causing a non-uniform fill in the vias shown in Fig. 1B.

Certainly, it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to form another metal layer in AAPA Fig. 1B, motivated by a need to complete the known and required electrical connections for the exemplary AAPA DRAM device depicted.

AAPA explains that these openings of different depths in AAPA Fig. 1B are difficult to fill reliably. Still referring to AAPA Fig. 1B, Wolf also teaches that the AAPA vias/plugs 9 and 12 at different depths in the figure are difficult to fill, which is a problem readily recognizable as comparable to the “price to be paid for planarization” of an interlevel dielectric such as AAPA layers 6 or 8 [see Section 4.4.1.3 of Wolf, Fig. 4-43]. “In such cases,” Wolf teaches, “it may be necessary to *avoid* the use of a complete planarization process...” [page 206, emphasis added]. Wolf teaches that holes of the same depth in an ILD (InterLevel Dielectric like AAPA layers 6 and 8) are easiest to fill, but when one requires all openings to be the same depth, the inherent uneven topology can hinder accurate photolithography. Wolf teaches a *tradeoff in planarity*.

Even with the problem of different depths noted, Wolf teaches that up to three levels of metal can be accommodated with *sloped* vias in a “smoothing” procedure, the sloped vias being desired for better step coverage [footnote under Fig. 4-13]. In view of Wolf’s teaching that up to 3 levels of metal can be accommodated with sloped vias using a “smoothing” in lieu planarization, it would have been obvious to one of ordinary skill in the art to use “smoothing” for AAPA layers 6 and 8 such that any holes formed in the layers would inherently be of “substantially the same depth” to ease quality filling of the openings [as in Fig. 4-9(b) of Wolf compared to AAPA Figs. 1A and 1B].

Applicant's claimed modification to the prior art includes a structural modification in adding "tapered upper portions" in the first AAPA layer 6 to "ensure alignment" of a second metal formed in holes of the second AAPA layer 8 [page 26, paper no. 15]. Yet, "having a tapered upper portion" and "wider at the top than at the bottom" do not distinguish in scope from the inherent nature of a dry-etched via plug.

For example, referring to Fig. 4-43a of Wolf, the drawing shows a straight vertical wall via, but the corresponding via of "the real world" shown in Fig. 4-43b is clearly *tapered and wider at the top*. The examiner emphasizes that "having a tapered upper portion" does not preclude having a tapered lowered portion. Thus, applicant's claim language "reads on" the inherent taper of a vertical wall via expected as is shown in Fig. 4-43b of Wolf.

Wolf also teaches that sloped vias are easier to fill with a metal deposition since the slope at the top of the via assists in obtaining quality "step coverage". It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to utilize a combination of wet and dry etch to get a via having a tapered upper portion to assist in obtaining better step coverage [footnote at bottom of page 205 in view of Fig. 3-14c on page 106, showing how to flare the mouth of the openings for better step coverage with photoresist, wet and dry etching, for example].

Even if one of ordinary skill in the art did not intentionally provide a "flare" at the mouth of the vias, a dry etch would inherently cause openings "having a tapered upper portion" and having "an upper portion wider than a lower portion" as is seen in Wolf's "real world" photograph.

It would have been obvious to one of ordinary skill in the art at the time of applicant's claimed invention to modify AAPA Figs. 1A and 1B in view of the teachings of Wolf since Wolf teaches up to 3 levels of metal can be formed keeping holes in each ILD "substantially equal in depth", with "smoothing" in lieu of planarization, with a deposition of metal after each ILD is formed having openings.

It would have been obvious to one of ordinary skill in the art at the time of applicant's claimed invention to perform a metal deposition immediately after the first ILD 6 is deposited with openings formed therein, as in Fig. 4-13a of Wolf. While this figure in Wolf depicts a second planarized layer, there "is a price to be paid" comprising opening of differing depths being more difficult to fill reliably. It would have been obvious to one of ordinary skill in the art to retain the conformal nature of both AAPA ILD layers 6 and 8 at the suggestion of Wolf who sets forth that up to 3 metal levels can be provided when retaining holes of substantially equal depth in each layer, if one can bear the non-planar topology. One of ordinary skill in the art would have been motivated to purposefully slope (provide taper) in the holes, as is taught by Wolf, to improve "step coverage" for a sputter and etch-back to form a layer being "grown over" and then "extending slightly beyond (by patterning)" as in a well known framing of vias for alignment corresponding to the 7000 angstrom and 13000 angstrom deep vias of Wolf's Fig. 4-13a. The examiner emphasizes that applicant's claim language does not preclude patterning after blanket metal deposition (as in a known "framed via").

Alternatively to “blanket deposition” with patterning to form framed vias, Gutierrez teaches forming tungsten selectively to be embedded in each ILD layer after each layer is formed and before the next ILD layer is formed. This way, the vias are of substantially the same depth in each layer of the multilevel-interconnect, easing the simultaneous fill without patterning as depicted in the cover figure of Gutierrez.

Gutierrez is silent with regard to a need to form holes “having a tapered upper portion” or forming holes with a “width wider at the top than at the bottom”, and, as pointed out by applicant, Gutierrez even depicts “tapering” as occurring somewhat randomly in the hand-drawn cover figure. However, as set forth by the examiner in view of SEM photograph in Fig. 4-43b of Wolf, all vertical walled vias have some inherent “taper at the top” and are inherently “wider at the top than at the bottom”.

It would have been obvious to use selective W CVD to form via plugs in each layer as is taught by Gutierrez. Alternatively, selective polysilicon deposition taught by Wolf could be used for interconnects to avoid tungsten operations. As taught by Gutierrez and Wolf, by keeping the layers conformal, opening depths in each layer are inherently of substantially the same depth, allowing them to be selectively filled without overflow problems depicted in Fig. 4-43a of Wolf, for example.

Claims 64-70, 72-80 and 82-88 [DEVICE Claims]

Applicant is reminded of the proper treatment of “product-by-process” claims [see MPEP 2113].

It would have been obvious to one of ordinary skill in the art at the time of applicant's claimed invention to form a device with interlevel interconnects, such as that of AAPA Figs. 1A and 1B, with ILD layers 1A and 1B formed conformally, at the suggestion of Wolf for up to 3 metal levels, to retain the benefit of opening of equal depth to ease filling the openings evenly.

It would have been obvious to one of ordinary skill in the art to complete the device shown in AAPA Fig. 1B by adding and patterning a second metal layer in the openings of the second ILD layer 8 to complete the required electrical connections of the AAPA DRAM structure. In completing the connections, the vias in the first ILD layer 6 would inherently have "taper at the upper portion" as set forth above in view of the "real world" taper of a so-called "vertical wall via".

Allowable Subject Matter

3. The following is a statement of reasons for the indication of allowable subject matter:

During the interview conducted December 10, 2001, as is documented by applicant in paper no. 15, the examiner generally agreed that the prior art does not fairly suggest or teach *a particular combination of limitations not exclusively claimed by applicant at this time:*

The prior art does not fairly suggest modifying AAPA Fig. 1A-1B to utilize a 2-step *selective* deposition at the suggestion of Gutierrez, wherein the openings in the first ILD layer 6 are "flared" only at the top without taper at the bottom.

While framed vias (by patterning) were known for alignment [Fisher et al., U.S. Patent 4,917,759, cols. 1-2], the prior art teaches that sloped vias are not needed for selective CVD. For example, U.S. Patent 5,162,261 documents the benefits of sloped vias (inherently having taper at the upper portion and a wider upper portion than lower portion), but also “teaches away” in that:

A more modern technique involves using CVD (chemical vapor deposition) tungsten in non-sloped vias through a planar interlevel insulator layer. While this method provides reliable contacts between interconnect layers, the machinery to perform this method costs in excess of one million dollars in many applications. [col. 1, lines 44-49].

Thus, applicant’s combination of *selective* CVD with straight-walled vias having substantially flared mouths gain a benefit in controlling overflow of the simultaneous selective deposition in the plurality of holes while also helping alignment of the second level without sacrificing device miniaturization from a via tapered from top to bottom.

Since a dry-etched vertical wall via inherently has a “tapered upper portion” as established by Wolf’s “real world” SEM photograph, applicant’s claims do not distinguish from inherent tapering of the prior art.

Response to Arguments

4. Applicant’s arguments with respect to claims 1-39, 41-43, 45-70, 72-80 and 82-88 have been considered but are moot in view of the new ground(s) of rejection.

5. Applicant’s arguments regarding the “taper” of the openings are moot in view of the inherency of taper established by the examiner in this paper. Applicant’s arguments pertaining to “grown over and extending slightly beyond” does not preclude patterning of a blanket-deposited layer as in the first level of the device depicted in Fig. 4-13a of Wolf.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fuller et al. (U.S. Patent 5,162,261) is cited for "teach away" from openings having a "flare" at the mouth when using selective CVD W [col. 1].

Fisher et al. (U.S. Patent 4,917,759) is cited for teaching alignment assistance by using "framed vias" to create a larger upper portion "nail head" [cols. 1-2].

The following patents discuss the sloping (tapering) of vias to improve step coverage:

Thane et al. (U.S. Patent 5,366,848), col. 1, line 65 to col. 2, line 14.

Blalock (U.S. Patent 5,320,981), col. 1, lines 20-41.

Takahumi et al. (U.S. Patent 4,999,318), col. 1, lines 9-24.

Wolf et al. (U.S. Patent 4,495,220), col. 1, line 67 to col. 2, line 12.

Berglund et al. (U.S. Patent 4,902,377), col. 1, line 39 to col. 2, line 21.

Wilson et al. (U.S. Patent 4,369,090), col. 1, lines 1-49.

The following non-patent literature is relevant:

Saia et al. and Lee et al. articles in the *J. Electrochem. Soc.* are cited for teaching concepts of multilevel-interconnect technology using both blanket and selective deposition of tungsten to form plugs separately or continuously with interconnect lines.

Wolf (page 106) is cited for teaching a contact hole formation using photoresist, wet and dry etching to form a contact opening having a flared mouth.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 703-308-1680. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ETP
March 10, 2002


EVAN PERT